New Current Programmed Pixel Circuit for Active-Matrix Organic Light-Emitting-Diode Displays


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ABSTRACT

A new current programmed pixel circuit for active-matrix organic light-emitting-diode displays (AMOLED) was developed by using low temperature polycrystalline silicon (LTPS) technology. The new pixel circuit adopted not only asymmetric current mirror to reduce pixel charging time but two storage capacitors to increase OLED current holding ratio. The proposed current programmed pixel circuit kept high aperture ratio of the pixel and accurate OLED current despite parasitic resistance of power lines. Therefore, this pixel circuit is suitable for large size and high resolution AMOLED displays.

INTRODUCTION

Among their many advantages, organic light-emitting-diode (OLED) displays are thin, lightweight, self-lighting, as well as have a high contrast ratio, wide viewing angle, and fast response time, explaining why they have received much attention now. The traditional current programming driving scheme is to produce a current which is the same as or proportional to the input data current to drive the OLED to give out light. The brightness of the OLED and the scale of pixel driving current are the linear relations [1]. The operation of the current programmed driving circuit can be divided into two stages. The first stage is to sample the scale of the input current of the pixel. The second stage is that the driving TFT reproduces the sampled current to drive the OLED. In the last few years, there are a lot of works have proposed the principles of the current programmed driving circuit. It effectively solves the dependence of the OLED current on the threshold voltage variation and the mobility variation of low temperature polycrystalline silicon (LTPS) thin-film-transistor (TFT) and parasitic resistance resulting from the circuit layout.

The current programmed pixel can be divided into two types, the current copy type [2]-[4], [8], [9] and the current mirror type [5]-[9]. The typical current mirror type pixel circuit is shown in Fig. 1. The main advantage of the current programmed pixels is that pixel-to-pixel variations of device parameters can be eliminated by letting OLEDs settle to the corresponding data currents. In this way, the current programming technique can generate uniform luminance throughout the whole panel. At present, current programming scheme still has drawbacks such as low pixel aperture ratio and long pixel charging time for low gray levels. Low aperture ratio of pixel causes low brightness and generally results from large storage capacitor in the pixel. For the bottom emissive panel, the storage capacitor consumes the area that OLED give out light. The large storage capacitor is also the reason why the charging time is long. These two problems are the primary obstacles for high-quality and high-resolution AMOLEDs. In this work, we propose a new current programmed pixel circuit, which not only decreases the size of the storage capacitor to overcome the above-mentioned problems, but also increases the holding ratio of the OLED driving current.

PROPOSED CURRENT PROGRAMMED PIXEL CIRCUIT

The new current mirror type pixel circuit is composed of 5 TFTs and 2 capacitors as shown in Fig. 2(a). M1, M2, and M3 are P-type TFTs. M4 and M5 are N-type TFTs. The capacitors, C1 and C2, are both storage capacitors. In detail, M4 and M5 are a pair of TFTs as a current mirror and M5 is the main...
driving transistor. There are four external signals, the power supply (VDD), the ground (GND), the scan line (Sn), and the data line (IDATA). The operation principle is as follows:

**The first stage: the sampling stage**

The timing diagram of the control signals of the proposed pixel circuit is displayed in Fig. 2(b). When scan signal Sn is at low state, M1~M3 are turned on and IDATA begin to charge capacitors C1 and C2 at interval T1. As charging is enough, M4 and M5 lead to on state and meantime M4 and M5 form a current mirror. The VDD supplies the current $I_{OLED}$ that will pour into OLED to give out light at this moment. The relationship between the input current and the driving current will be

$$I_{DATA} = m \times I_{OLED},$$

(1)

Where $m$ is the proportion of aspect ratios of M4 to M5. C1 and C2 will keep almost the same potential, which is corresponding to the gate-to-source voltage of the main driving TFT and set by data current as the following equation.

$$V_{C1} = V_{C2} = V_{GS1} = \sqrt{\frac{2I_{data}}{\beta} + V_{th1}}$$

(2)

Where $V_{th1}$ is the threshold voltage of M1 and $\beta$ is a constant including the channel length $L$, the channel width $W$, the capacitance per unit area $C_i$, and the carrier mobility $\mu$, and is given by

$$\beta = \mu \times C_i \times \left( \frac{W}{L} \right)_{M1}.$$ 

(3)

**The second stage: the reproduction stage**

When scan signal Sn becomes at high state, M1~M3 are all leading to off state at interval T2, and the voltage stored in capacitor C2 drives M5 on and the OLED give out light continuously at this moment. Notably, the OLED current is independent of the threshold voltage and the field-effect mobility of the driving transistor and is determined by the input data current and the aspect ratio of M4/M5, as predicted by (1). Because the voltages on capacitors C1 and C2 are almost the same, it makes drain and source of M3 being the same electric potential. Hence, the drain-to-source leakage current of M3 will be extremely low. On the other hand, M2 is also at off state and its drain-to-source leakage current is low. It guarantees the voltage on capacitor C1 will not drop too fast. Therefore, the voltage at the gate of M5 remains stable, and the current $I_{OLED}$ maintains almost the same current in one frame period (~ 16.6 ms). By utilizing two identical capacitors to store the gate-to-source voltage of the driving transistor, it decreases the leakage current of the switching transistor, M3, so the sizes of the storage capacitors can be further reduced. Although there is more one storage capacitor in this pixel circuit than that in traditional one, the storage capacitors C1 and C2 can be significantly reduced. Therefore, the area taken up by the storage capacitors is still smaller than that in traditional one. The smaller storage capacitor area, the larger aperture ratio of the pixel is. The lower leakage current of M3, the higher voltage ($V_{GS}$) or current ($I_{DS}$) holding ratios is.

The main benefits of the presented pixel circuit are to decrease the storage capacitor and the leakage current of the switching TFT. Thus, the aperture ratio and the holding ratio of the OLED current are increased. In addition, the pixel charging time could be decreased due to small storage capacitor. The efficiency of light emission could be enhanced and power consumption could be decreased.

![Fig. 2](image-url)
SIMULATION RESULTS AND DISCUSSIONS

Settling Time

The main drawback of the traditional current programmed pixel circuit is that the pixel charging time is too long. Especially for the current copy type driving circuit, because the driving current is only few nA at the lowest gray level, it has a long settling time for charging the storage capacitor of the pixel and the parasitic capacitance of the data line. It is believed that the current copy type pixel circuit is not suitable for large-size and high-resolution displays. However, the current mirror type pixel circuit can adopt asymmetric TFT devices in the current mirror and increase the ratio of I_{DATA} to I_{OLED}, as expressed by (1). Therefore, the settling time can be effectively reduced.

Figure 3 exhibits the simulation results of the data current as a function of the pixel charging times for different aspect ratio of TFTs in the current mirror type pixel circuit. This simulation sets the OLED current at about 8 nA for the lowest gray level. The new programmed pixel circuit is designed to 1:1 or m:1 current mirrored pixel circuit. For 1:1 current mirrored pixel circuit, the charging time of pixel circuit is 27.2 us for the charging ratio of 99.23%, which is equivalent to 5 RC (time constant). For 5:1 current mirrored pixel circuit. The result shows that when I_{DATA} is 40 nA, the charging time decreases to 6.47 us, which is almost a quarter compared to that in the 1:1 current mirrored case. Therefore, it is better to use m:1 current mirror in the pixel as driving high-resolution panels.

Current Holding Ratio

Except the charging ratio, the voltage holding ratio on the storage capacitor or the current holding ratio of I_{OLED} is another important factor to influence the accuracy of the luminance of the pixel. In order to study the effects of the voltage holding ratio on the storage capacitor, the developed current programmed pixel circuit and the pixel in [5] were simulated and compared. Table I lists the size of all components for these two pixel circuits for SPICE simulation. As can be seen from table I, each storage capacitor in the proposed circuit is a half of that in [5]. Thus, the area occupied by the two capacitors is similar to that in [5]. As to TFTs, the proposed circuit has one more transistor. Based on layout experience, the area of the TFT is much smaller than that of the capacitor. Therefore, these two pixels have approximate aperture ratios.

Figure 4 presents the OLED current as a function of the holding time for the proposed pixel circuit with a total storage capacitor of 0.5 pF and the conventional pixel circuit in [5] with storage capacitors of 0.5 pF and 5 pF. Form Fig. 4, the OLED current of pixel with C_S = 0.5 pF in [5] drops from 5 uA to 4.238 uA or 15.2 % in a frame time (~ 16.6 ms). The OLED current with C_S = 5 pF in [5] drops from 5 uA to 4.91 uA or 1.8 %. On the contrary, the driving current of the proposed pixel circuit drops from 5 uA to 4.94 uA or 1.2 %. It is found that the pixel circuit in [5] has a large storage capacitor (5 pF), but its current degradation in a frame time still exceeds that of the proposed pixel circuit with a small storage capacitor (0.5 pF). The proposed pixel circuit has not only higher current holding ratio but much smaller storage capacitor size than the conventional one. That is, the proposed current programmed pixel circuit has higher aperture ratio, thus higher and more accurate brightness than the conventional one.

Parasitic Resistance

The parasitic effect of the signal line is one of the major factors to influence the display quality. For example, parasitic resistance of the power line degrades the supply voltage and then results in incorrect luminance of gray levels on OLEDs. Figure 5 shows the parasitic resistance effect on the OLED current for the proposed pixel circuit. Considering the parasitic resistances of 0-5 kΩ series connected with power supply (VDD), the OLED current drops from 4.9995 uA to 4.9935 uA, and the maximum error in the OLED current is only -0.12 %, which is a very small value and cannot be observed by human eyes. Compared to conventional voltage programmed pixel circuit, the proposed one has a stable OLED current, which is not influenced by the parasitic resistance, is favorable for large size AMOLEDs.

CONCLUSION

The new current-programmed pixel circuit was developed by utilizing five transistors and two storage capacitors for AMOLEDs. The presented pixel circuit features high pixel aperture ratio, short charging time, and high current holding ratio. Besides, the OLED current is independent of threshold voltage and field-effect mobility of TFTs, and parasitic resistance of power lines. Therefore the new current-programmed pixel circuits can be applied for large size, high resolution and high quality AMOLEDs.

ACKNOWLEDGMENTS

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REFERENCES
Fig. 3 The simulation results of the data current as a function of pixel charging times for different aspect ratio of TFTs in the current mirror type pixel circuit.

Fig. 4 The OLED current as a function of the holding time.

Fig. 5 The parasitic resistance effect on the OLED current for the proposed pixel circuit.

TABLE I

| Design parameters of the proposed pixel circuit and the pixel circuit in [5] for SPICE simulation |
|----------------|----------------|----------|--------|
| Pixel circuit in [5] | T2~T4 | T1 | C |
| | 4um/4um | 20um/4um | 500 fF |
| Proposed pixel circuit | M1~M3 · M5 | M4 | C1 · C2 |
| | 4um/4um | 20um/4um | 250 fF |