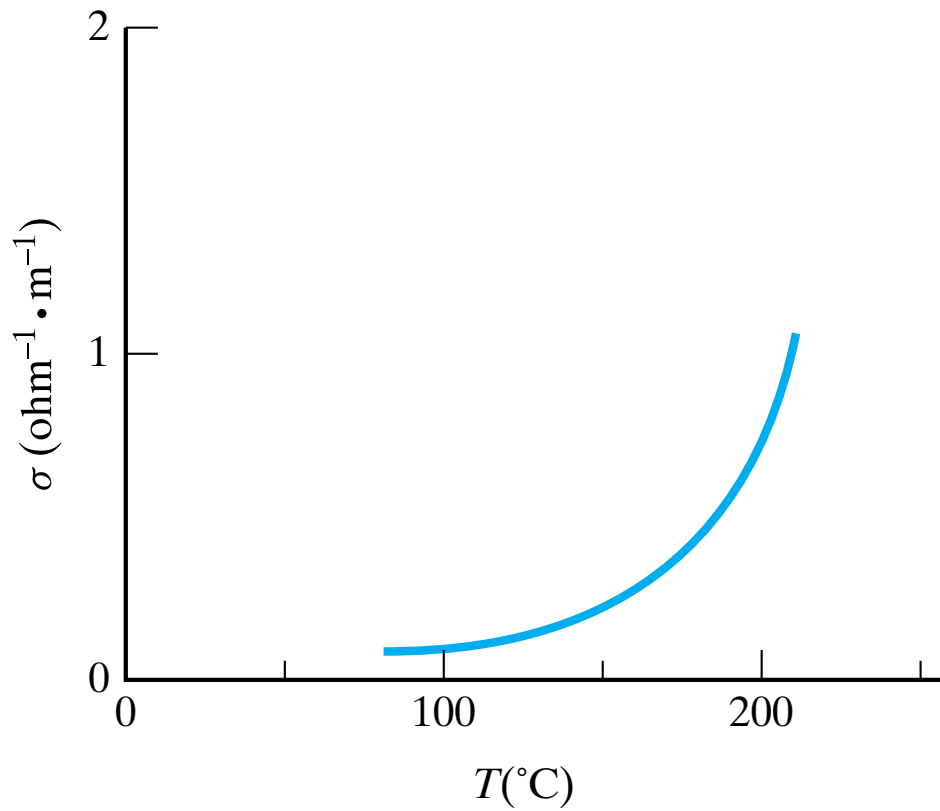


# CHAPTER 17

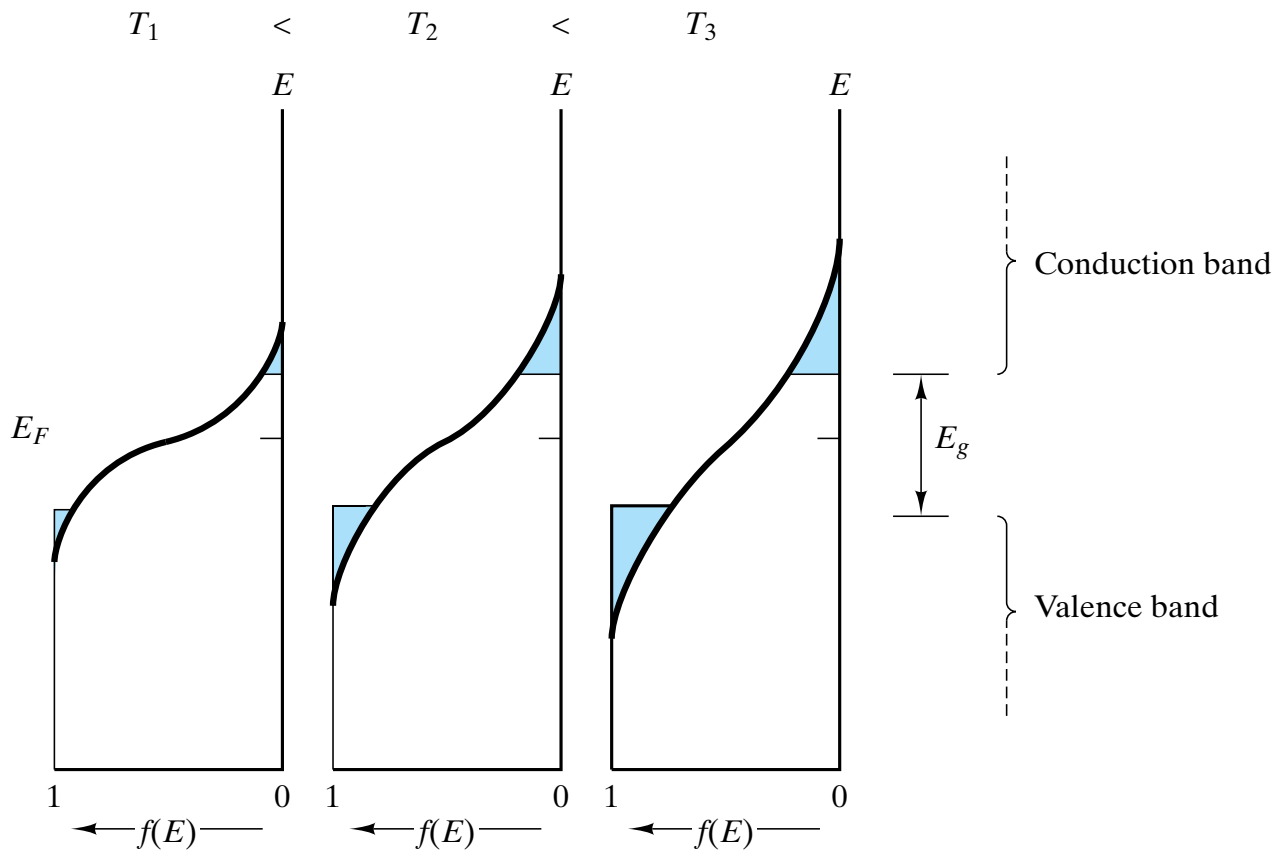
## Semiconductor Materials



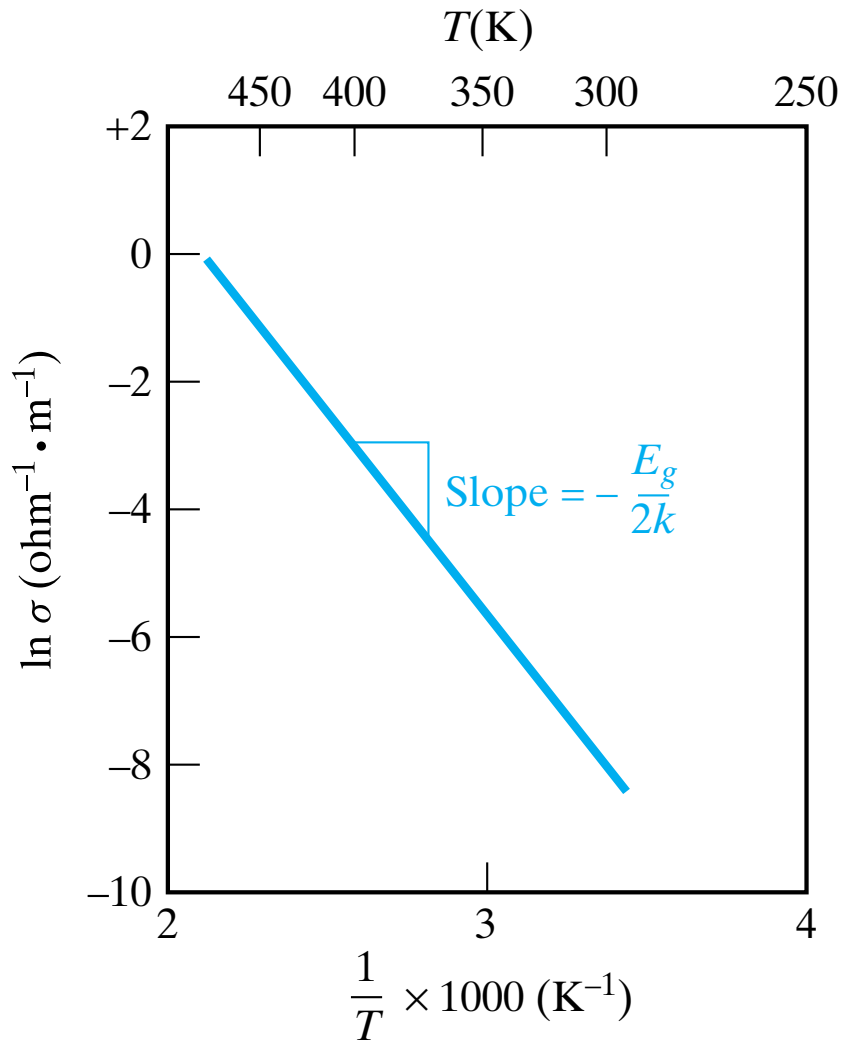
*The modern microprocessor is a state-of-the-art application of semiconductor materials encased in a package of conventional structural materials. This 500 MHz processor contains 10 million transistors on a single silicon chip. (Courtesy of Intel.)*



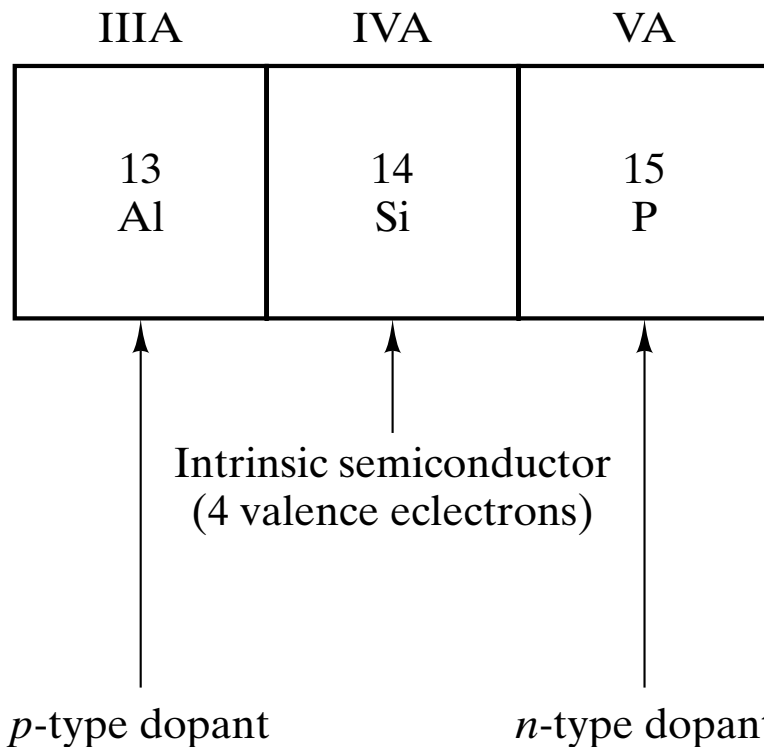
**Figure 17-1** Variation in electrical conductivity with temperature for semiconductor silicon. Contrast with the behavior shown for the metals in Figure 15–10. (This plot is based on the data in Table 17.1 using Equations 15.14 and 17.2.)



**Figure 17-2** Schematic illustration of how increasing temperature increases overlap of the Fermi function,  $f(E)$ , with the conduction and valence bands giving increasing numbers of charge carriers. (Note also Figure 15-9.)



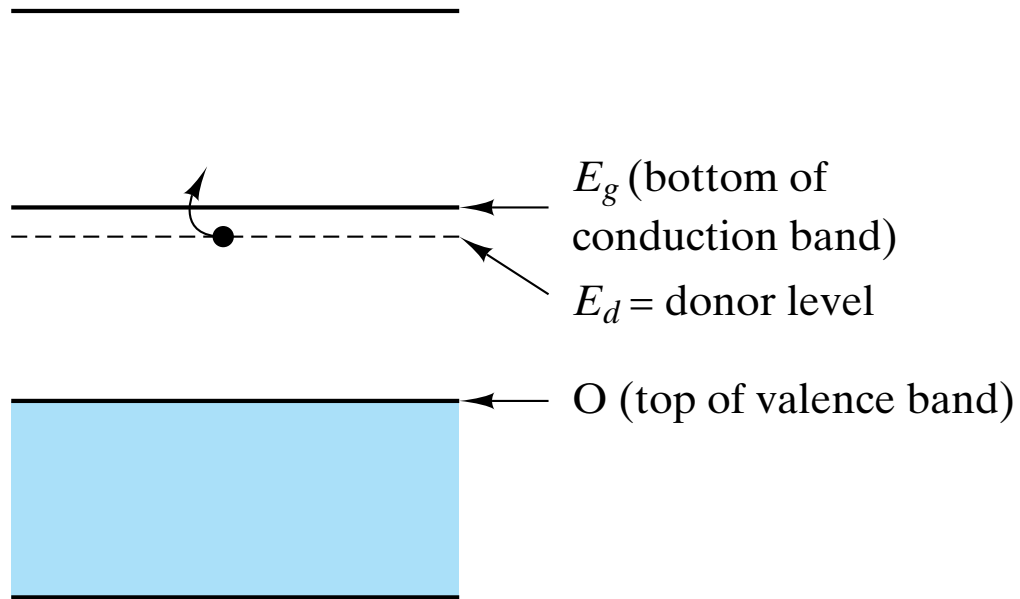
**Figure 17-3** Arrhenius plot of the electrical conductivity data for silicon given in Figure 17-1. The slope of the plot is  $-E_g/2k$ .



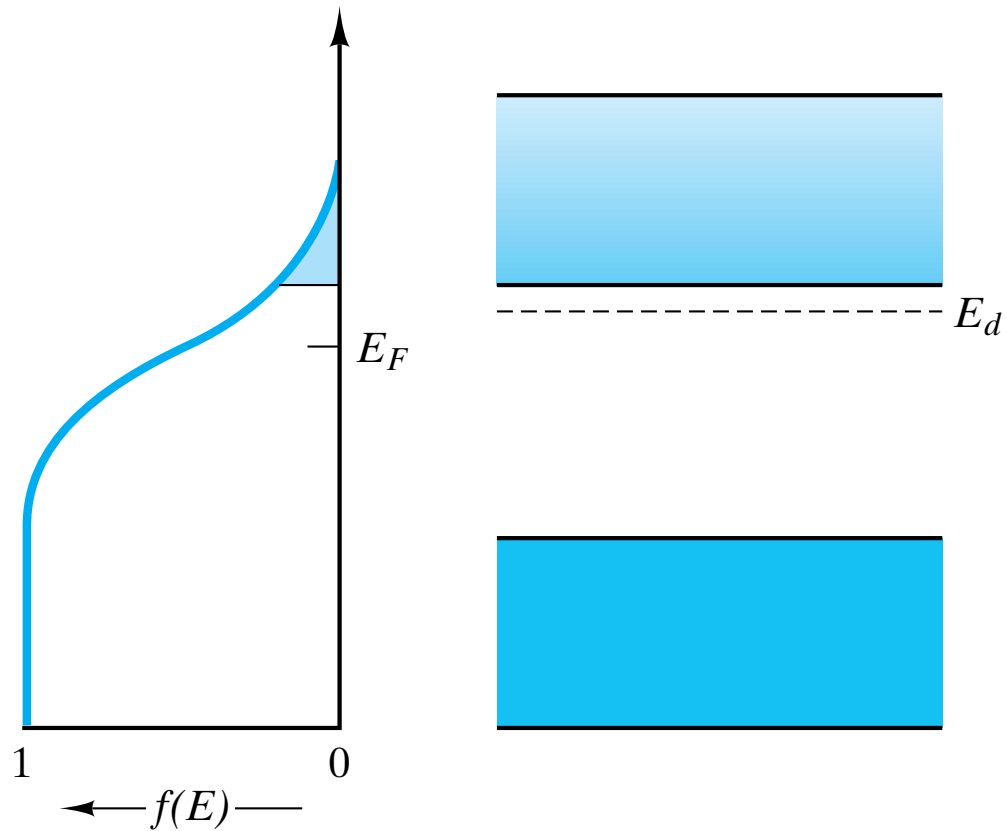
(only 3 valence electrons →  
electron hole or positive  
charge carrier )

(5 valence electrons →  
conduction electron or  
negative charge carrier )

**Figure 17-4** *Small section of the periodic table of elements. Silicon, in group IVA, is an intrinsic semiconductor. Adding a small amount of phosphorus from group VA provides extra electrons (not needed for bonding to Si atoms). As a result, phosphorus is an n-type dopant (i.e., an addition producing negative charge carriers). Similarly, aluminum, from group IIIA, is a p-type dopant in that it has a deficiency of valence electrons leading to positive charge carriers (electron holes).*

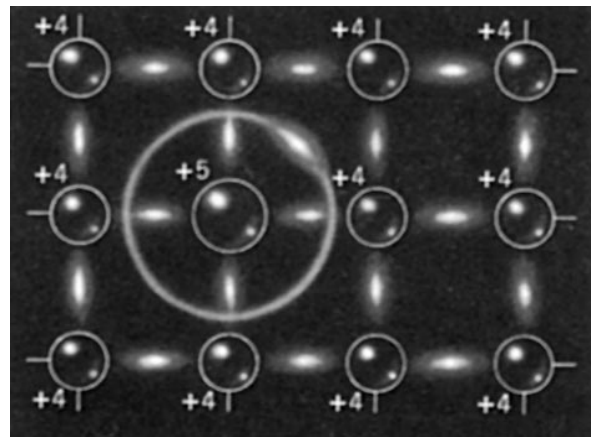


**Figure 17-5** Energy band structure of an n-type semiconductor. The extra electron from the group VA dopant produces a donor level ( $E_d$ ) near the conduction band. This provides relatively easy production of conduction electrons. This figure can be contrasted with the energy band structure of an intrinsic semiconductor in Figure 15-9.

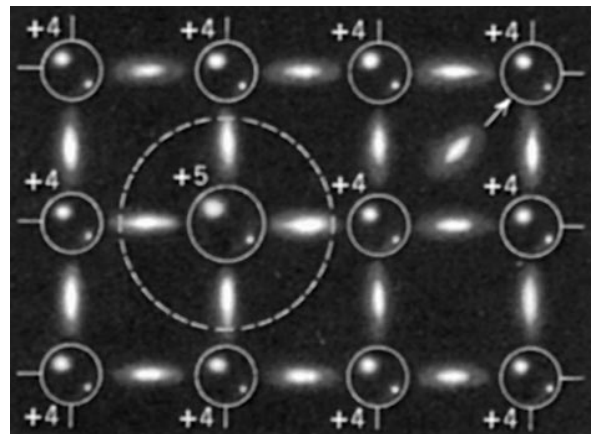


**Figure 17-6** Comparison of the Fermi function,  $f(E)$ , with the energy band structure for an n-type semiconductor. The extra electrons shift the Fermi level ( $E_F$ ) upward compared to Figure 15-9 (where it was in the middle of the band gap for an intrinsic semiconductor).

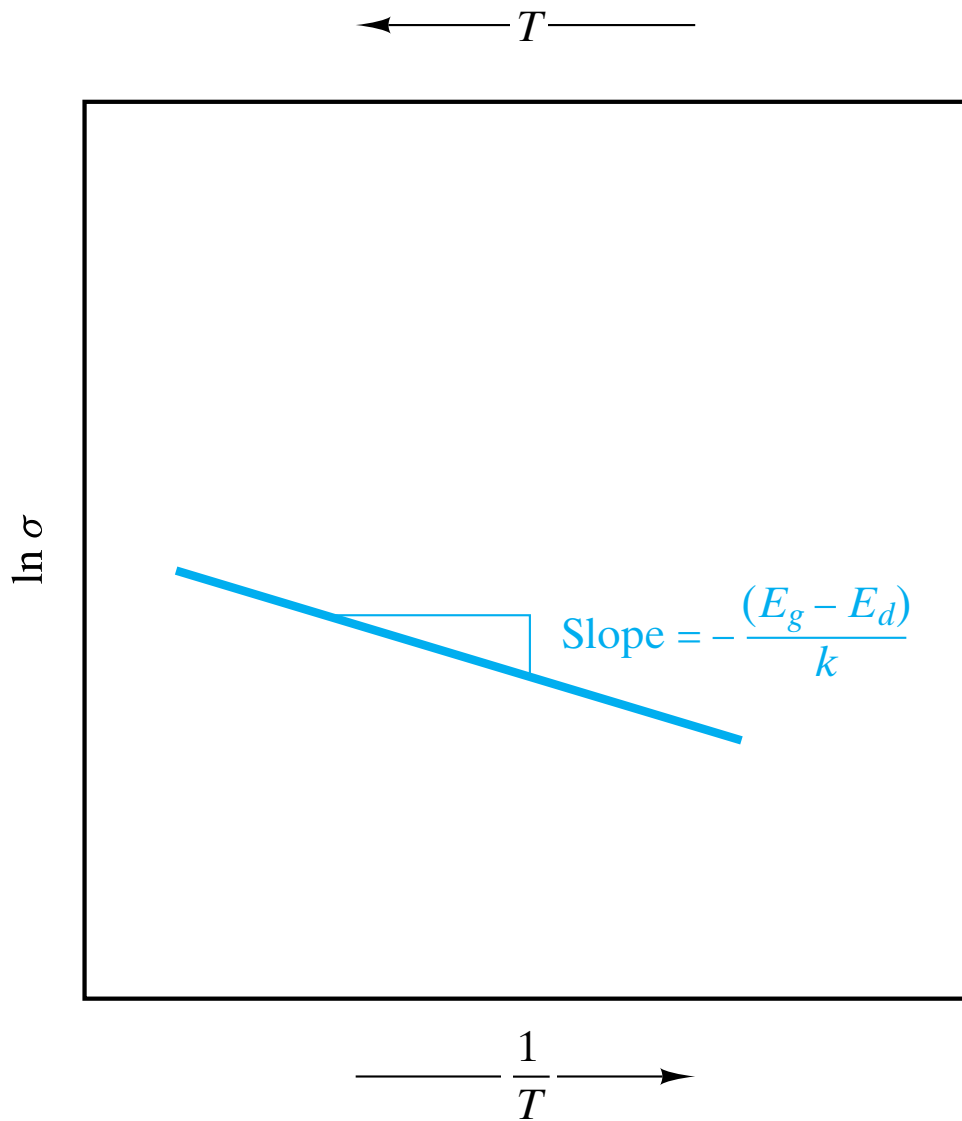
**Figure 17-7** Schematic of the production of a conduction electron in an n-type semiconductor. (a) The extra electron associated with the group VA atom can (b) easily break away, becoming a conduction electron and leaving behind an empty donor state associated with the impurity atom. This can be contrasted with the similar figure for intrinsic material in Figure 15-27. (From R. M. Rose, L. A. Shepard, and J. Wulff, *The Structure and Properties of Materials, Vol. 4: Electronic Properties*, John Wiley & Sons, Inc., New York, 1966.)



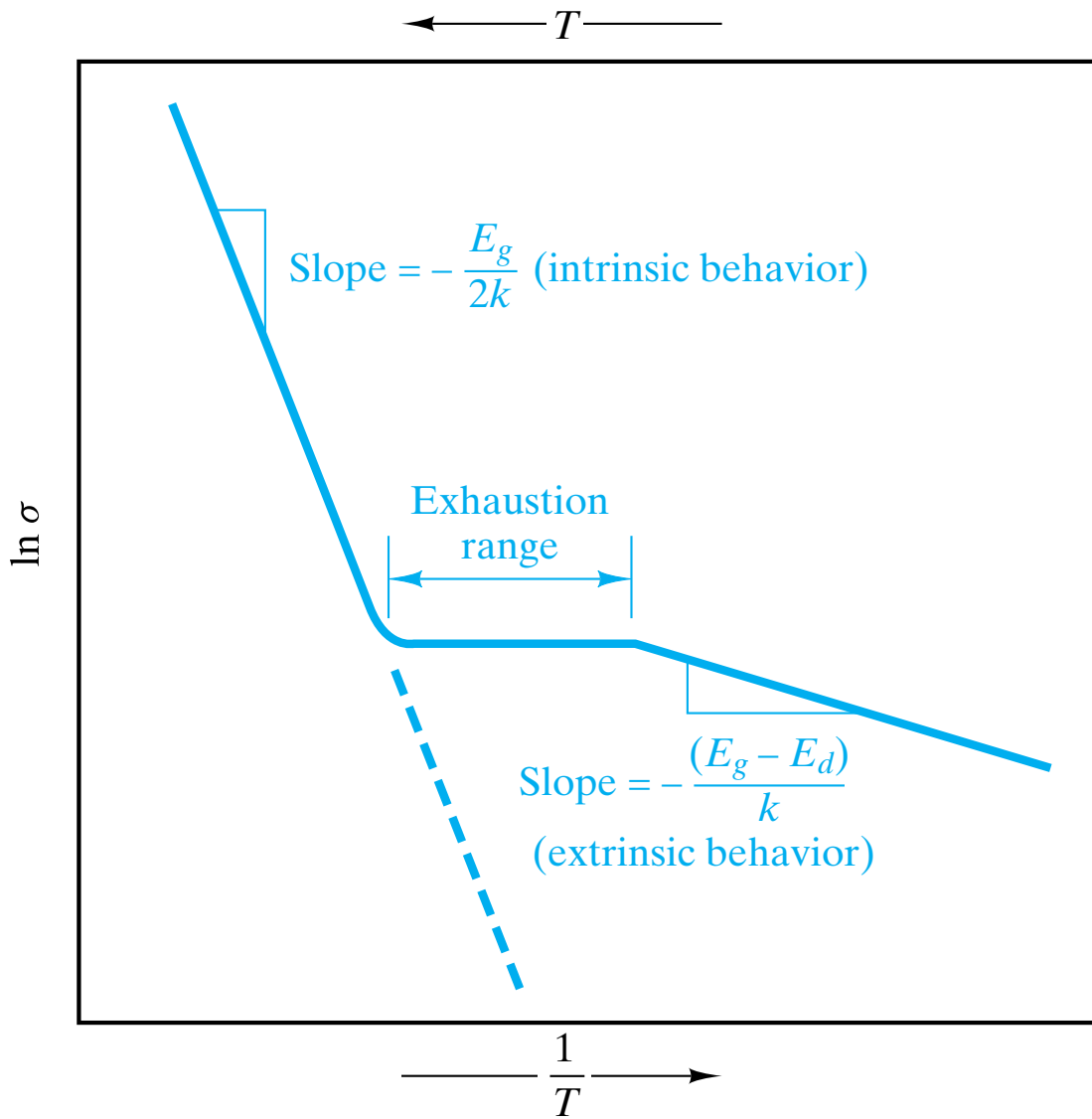
(a)



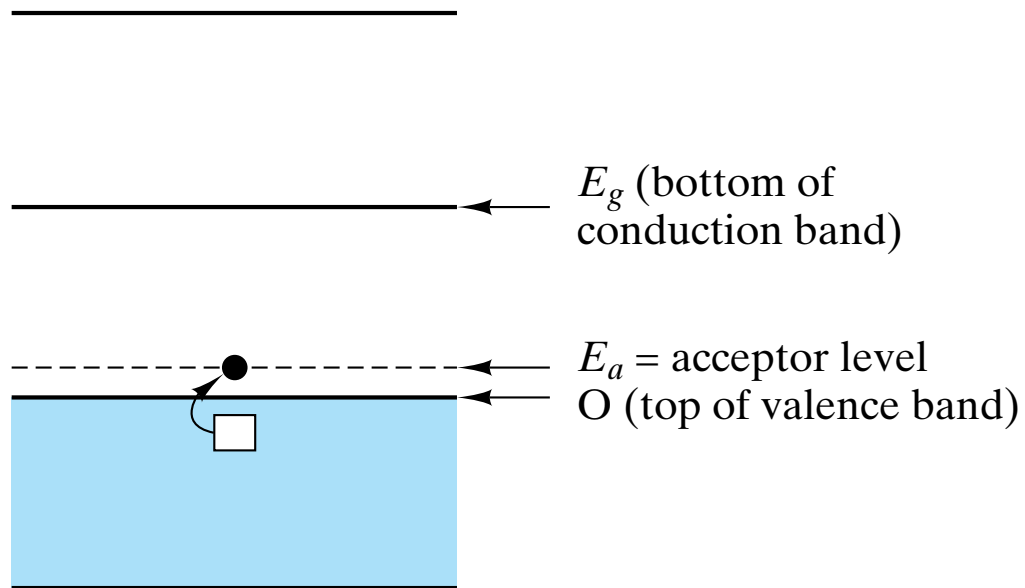
(b)



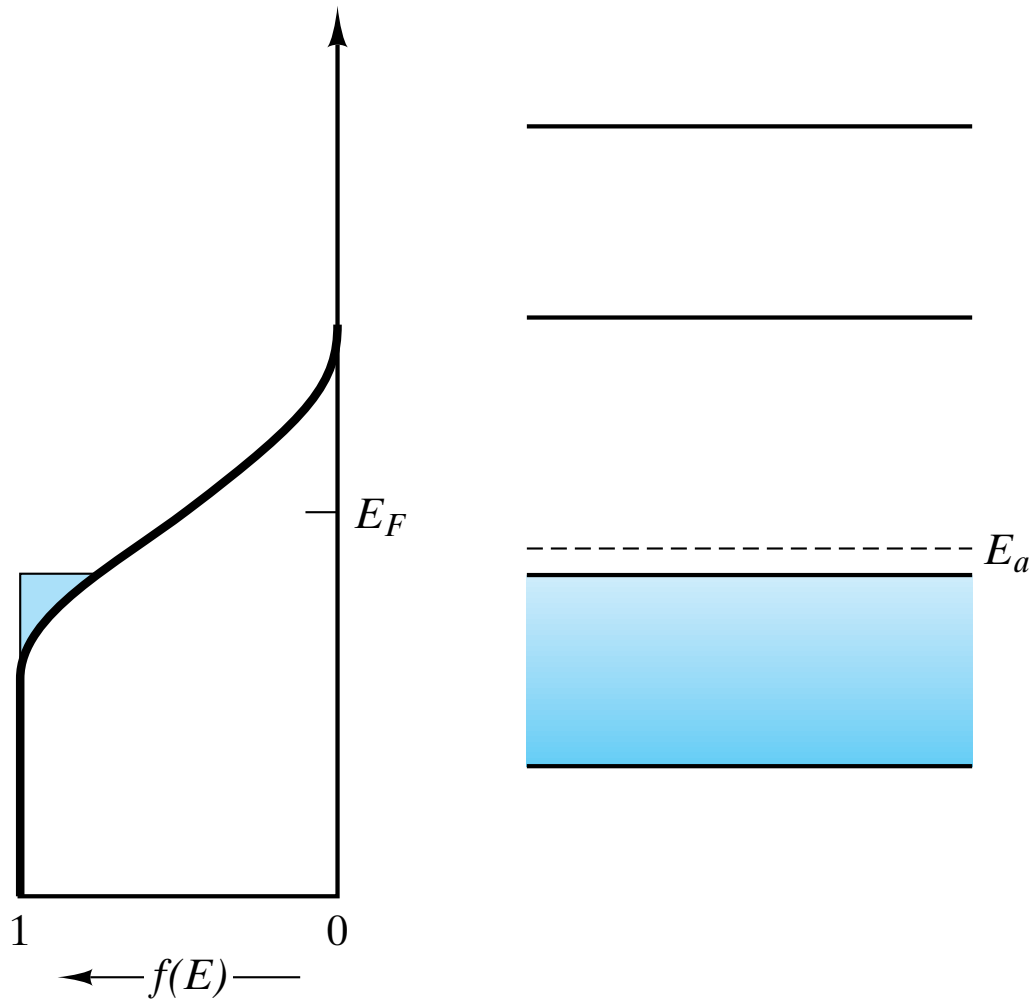
**Figure 17-8** Arrhenius plot of electrical conductivity for an *n*-type semiconductor. This can be contrasted with the similar plot for intrinsic material in Figure 17-3.



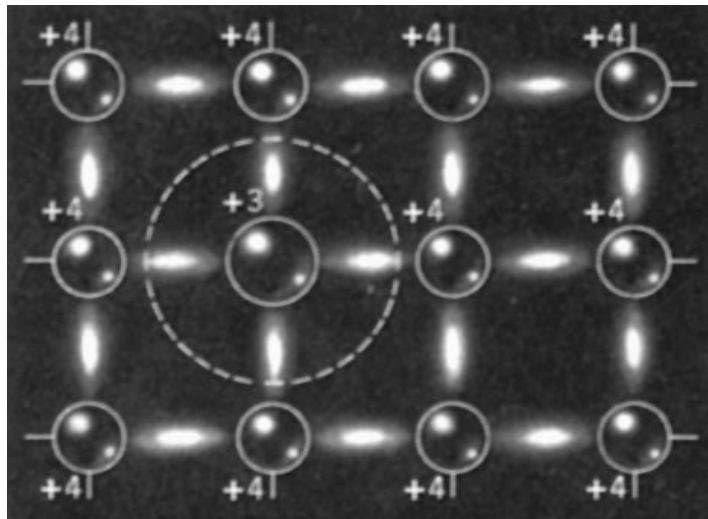
**Figure 17-9** Arrhenius plot of electrical conductivity for an n-type semiconductor over a wider temperature range than shown in Figure 17-8. At low temperatures (high  $1/T$ ), the material is extrinsic. At high temperatures (low  $1/T$ ), the material is intrinsic. In between is the exhaustion range, in which all “extra electrons” have been promoted to the conduction band.



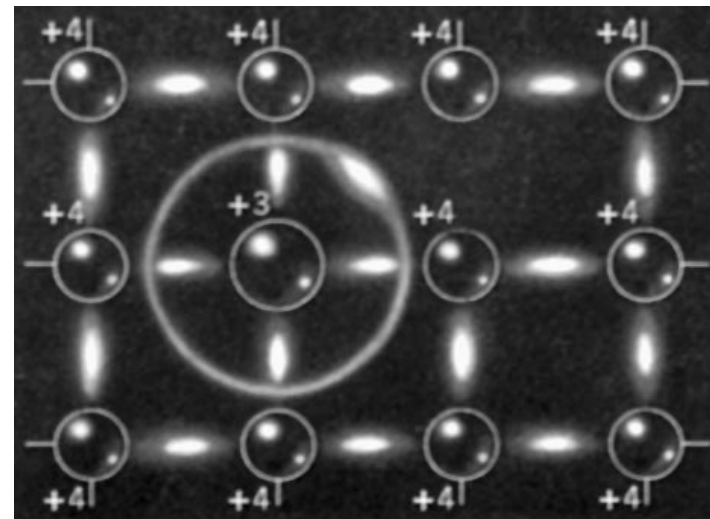
**Figure 17-10** *Energy band structure of a p-type semiconductor. The deficiency of valence electrons in the group IIIA dopant produces an acceptor level ( $E_a$ ) near the valence band. Electron holes are produced as a result of thermal promotion over this relatively small energy barrier.*



**Figure 17-11** Comparison of the Fermi function with the energy band structure for a *p*-type semiconductor. This electron deficiency shifts the Fermi level downward compared to Figure 15-9.

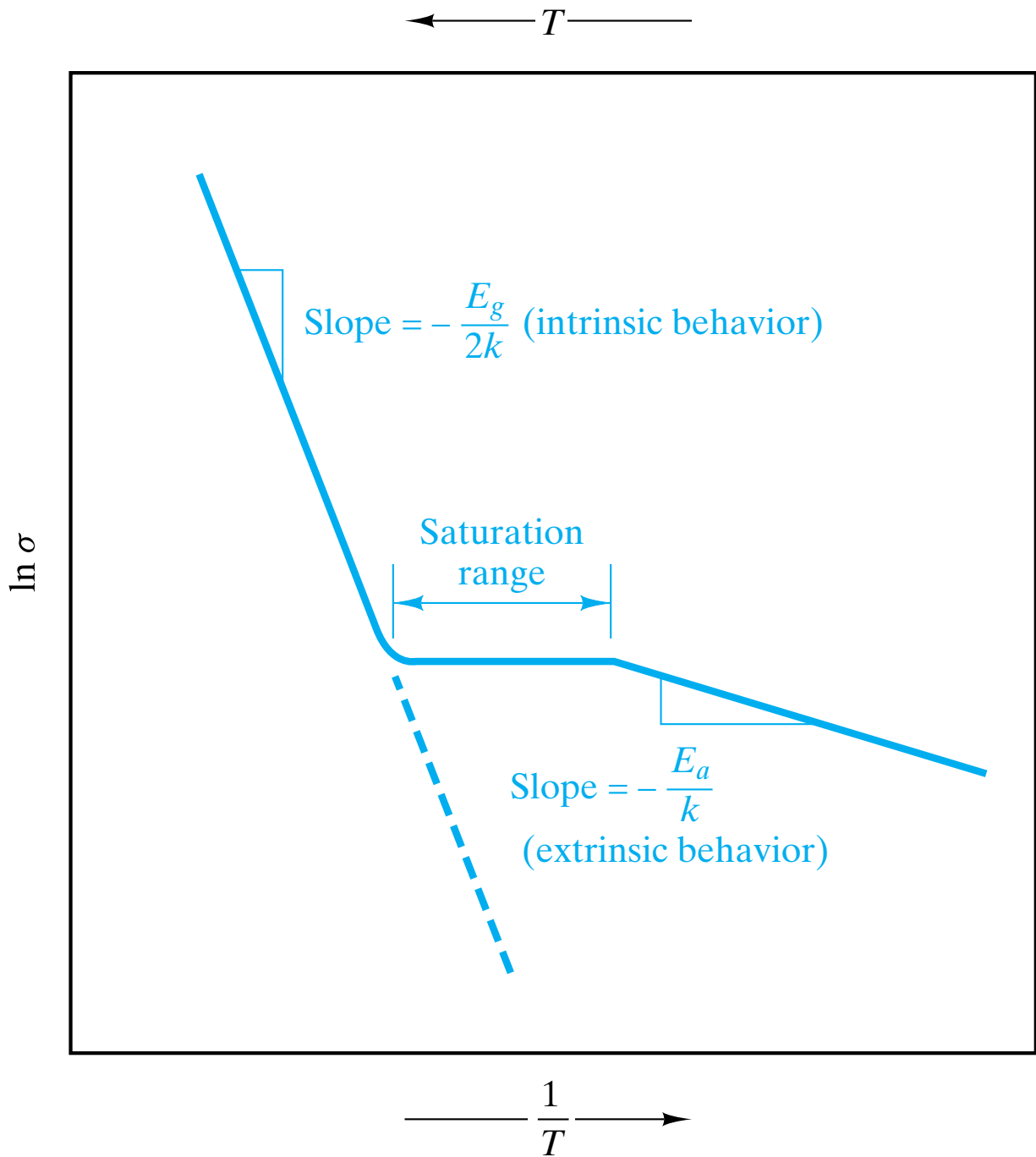


(a)

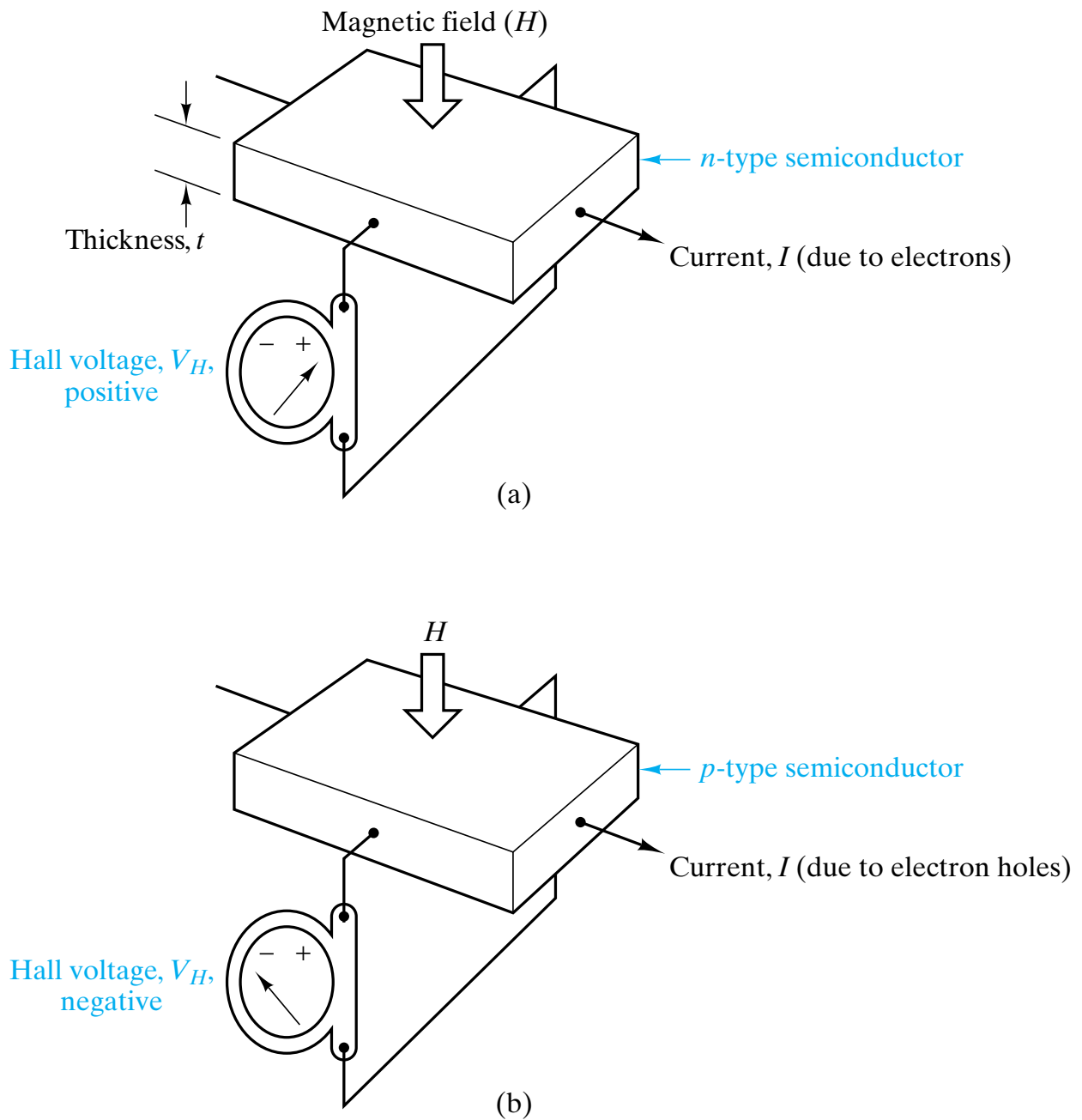


(b)

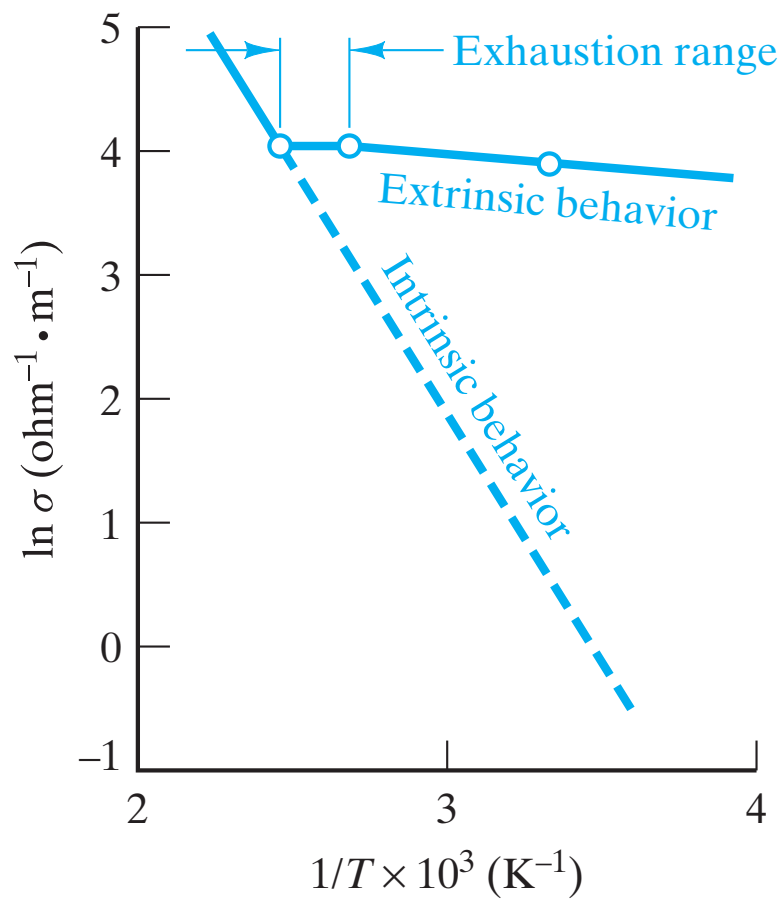
**Figure 17-12** Schematic of the production of an electron hole in a *p*-type semiconductor. (a) The deficiency in valence electrons for the group IIIA atom creates an empty state, or electron hole, orbiting about the acceptor atom. (b) The electron hole becomes a positive charge carrier as it leaves the acceptor atom behind with a filled acceptor state. (The motion of electron holes, of course, is due to the cooperative motion of electrons.) (From R. M. Rose, L. A. Shepard, and J. Wulff, *The Structure and Properties of Materials, Vol. 4: Electronic Properties*, John Wiley & Sons, Inc., New York, 1966.)

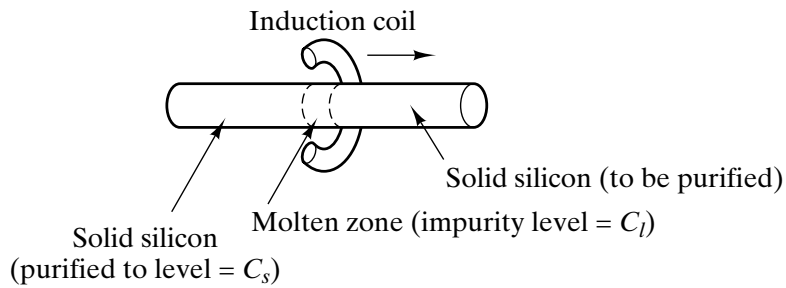


**Figure 17-13** Arrhenius plot of electrical conductivity for a p-type semiconductor over a wide temperature range. This is quite similar to the behavior shown in Figure 17-9. The region between intrinsic and extrinsic behavior is termed the saturation range corresponding to all acceptor levels being “saturated” or occupied with electrons.



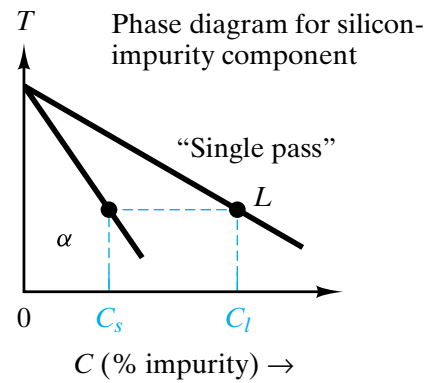
**Figure 17-14** The application of a magnetic field (with field strength,  $H$ ), perpendicular to a current,  $I$ , causes a sideways deflection of charge carriers and a resulting voltage,  $V_H$ . This phenomenon is known as the Hall effect. The Hall voltage is given by Equation 17.8. For (a) an n-type semiconductor, the Hall voltage is positive. For (b) a p-type semiconductor, the Hall voltage is negative.



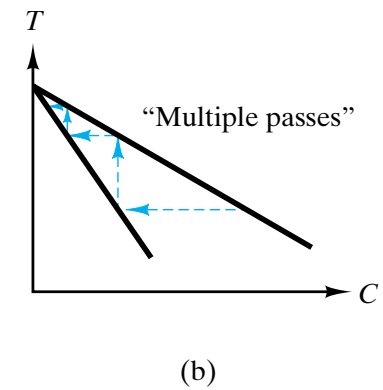


Segregation coefficient =

$$K = \frac{C_s}{C_l}$$

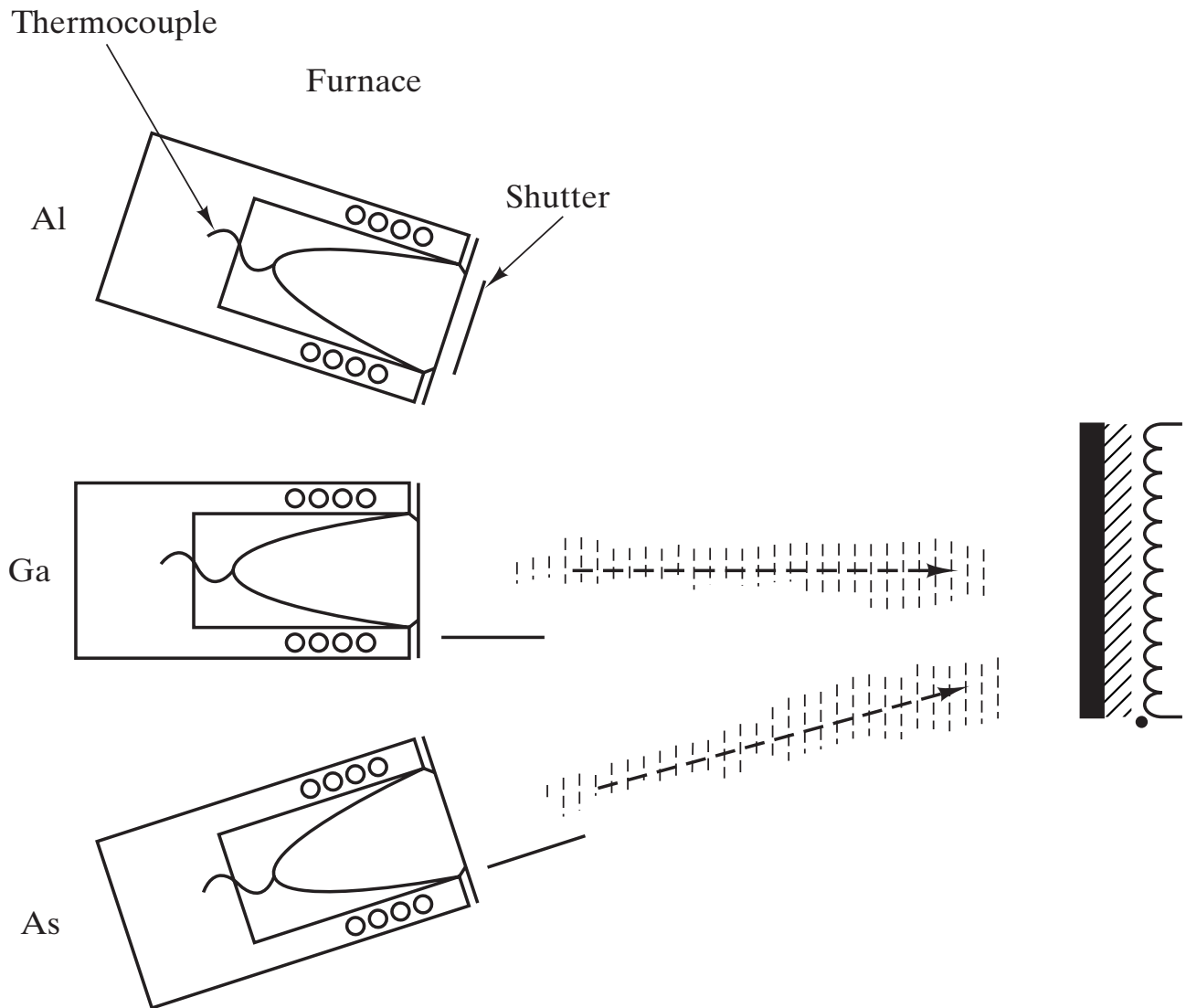


(a)

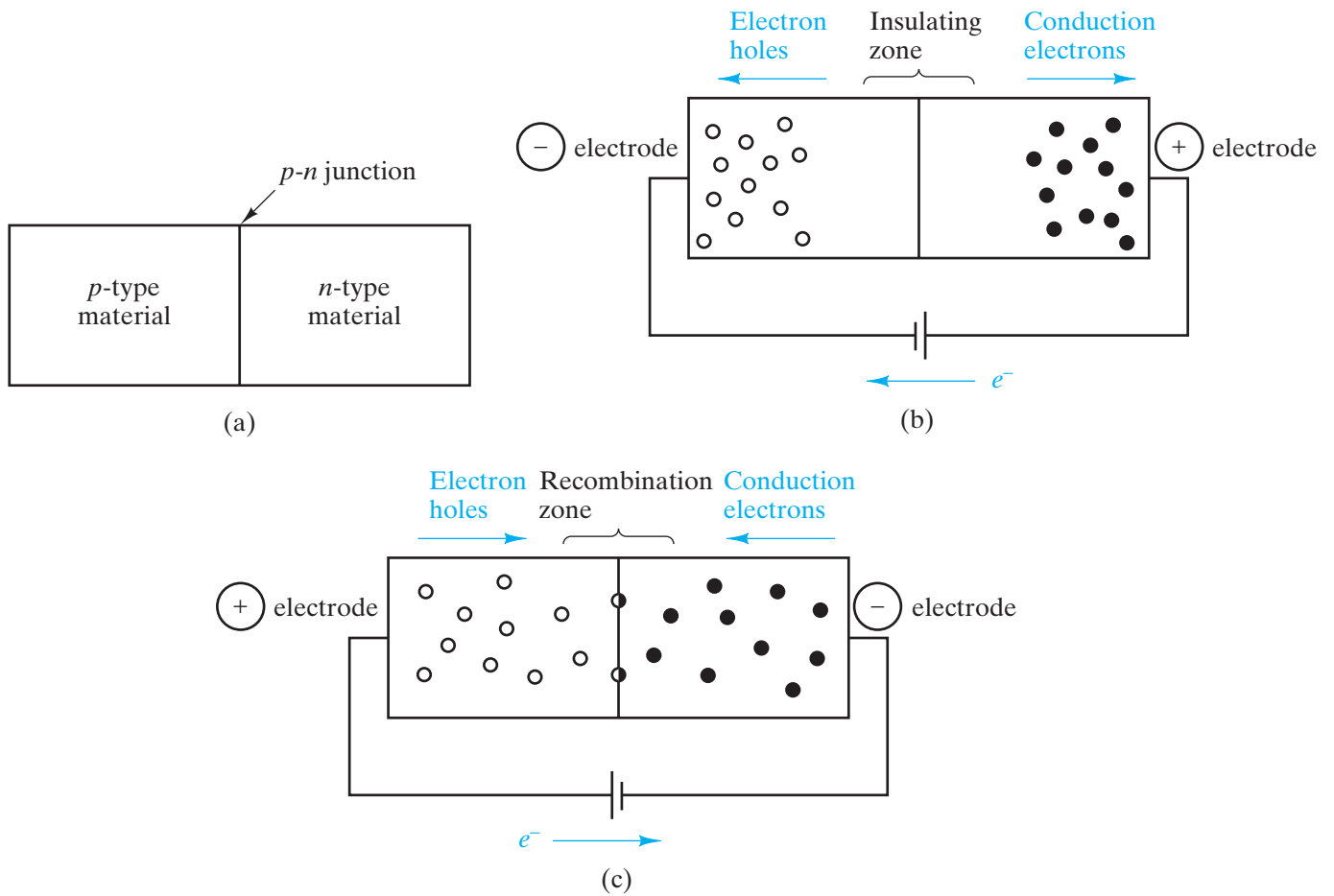


(b)

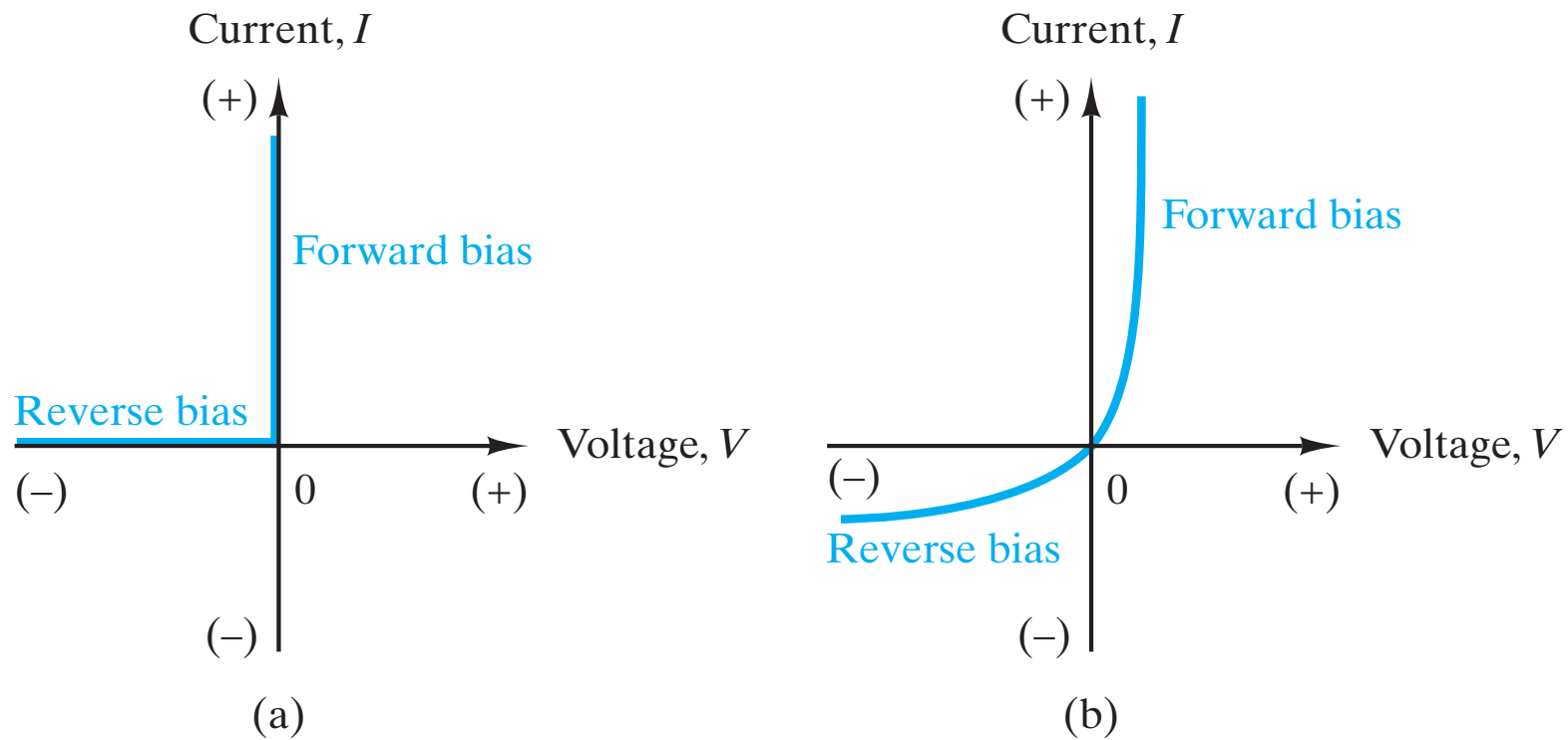
**Figure 17-15** In zone refining, (a) a single pass of the molten “zone” through the bar leads to the concentration of impurities in the liquid. This is illustrated by the nature of the phase diagram. (b) Multiple passes of the molten zone lead to increasing purification of the solid.



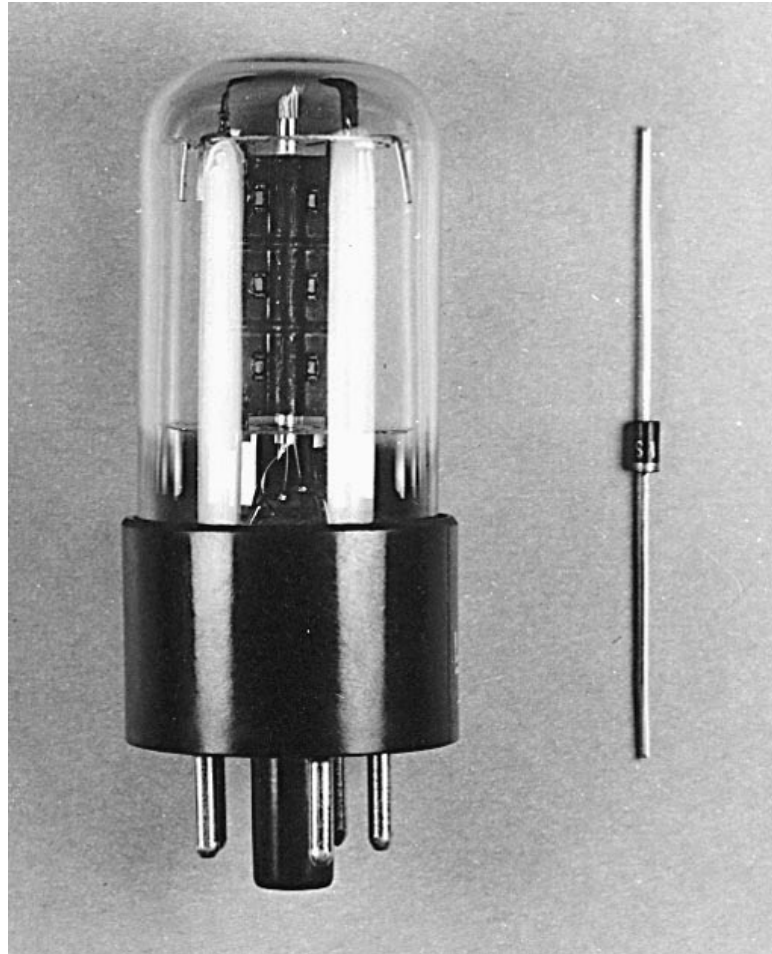
**Figure 17-16** Schematic illustration of the molecular-beam epitaxy technique. Resistance-heated source furnaces (also called effusion or Knudsen cells) provide the atomic or molecular beams (approximately 10-mm radius). Shutters control the deposition of each beam onto the heated substrate. (From J. W. Mayer and S. S. Lau, *Electronic Materials Science: For Integrated Circuits in Si and GaAs*, Macmillan Publishing Company, New York, 1990.)



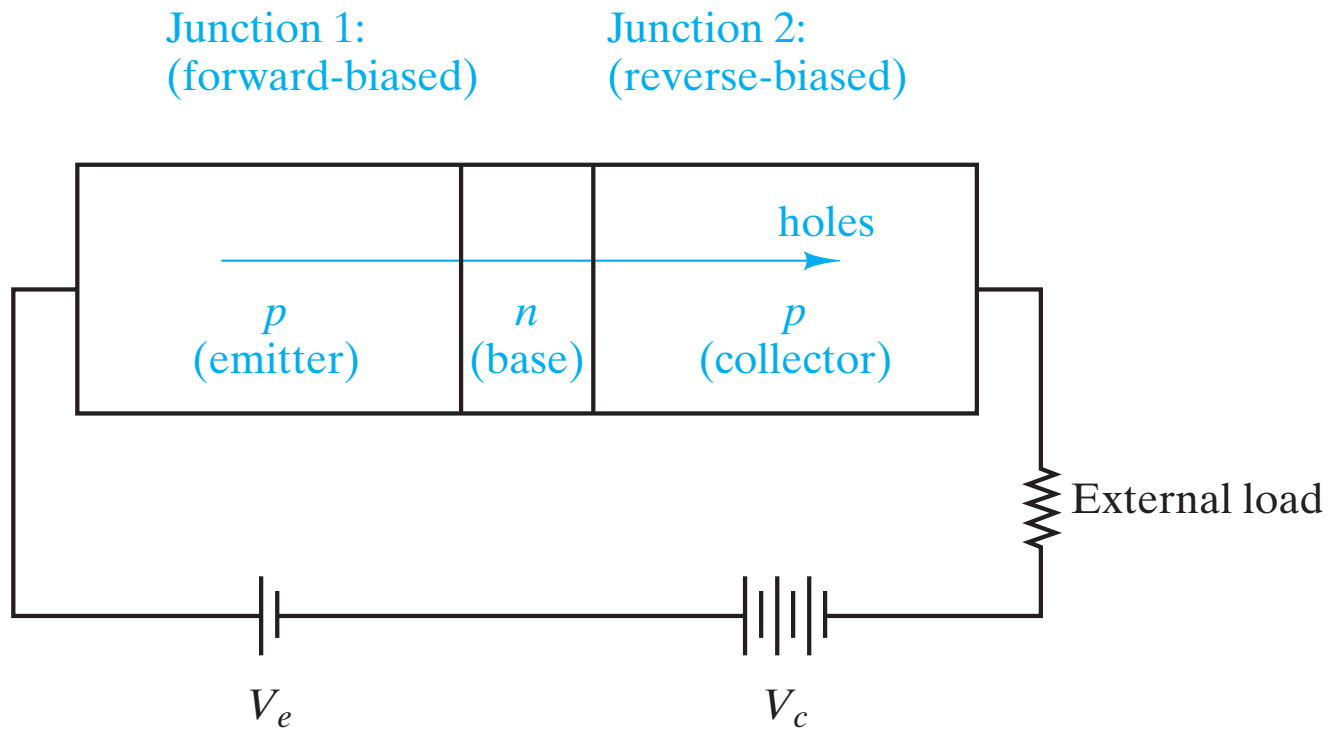
**Figure 17-17** (a) A solid-state rectifier, or diode, contains a single  $p$ - $n$  junction. (b) In reverse bias, polarization occurs and little current flows. (c) In forward bias, majority carriers in each region flow toward the junction, where they are continuously recombined.



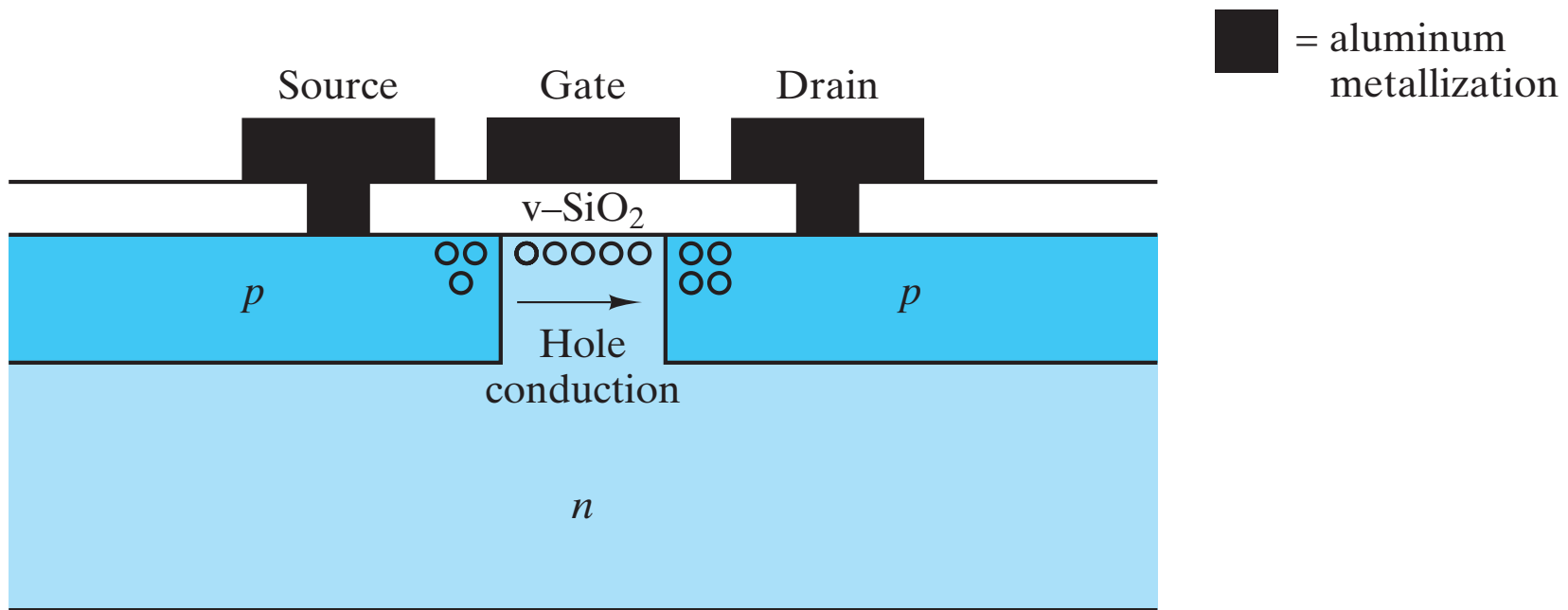
**Figure 17-18** Current flow as a function of voltage in (a) an ideal rectifier and (b) an actual device such as that shown in Figure 17-17.



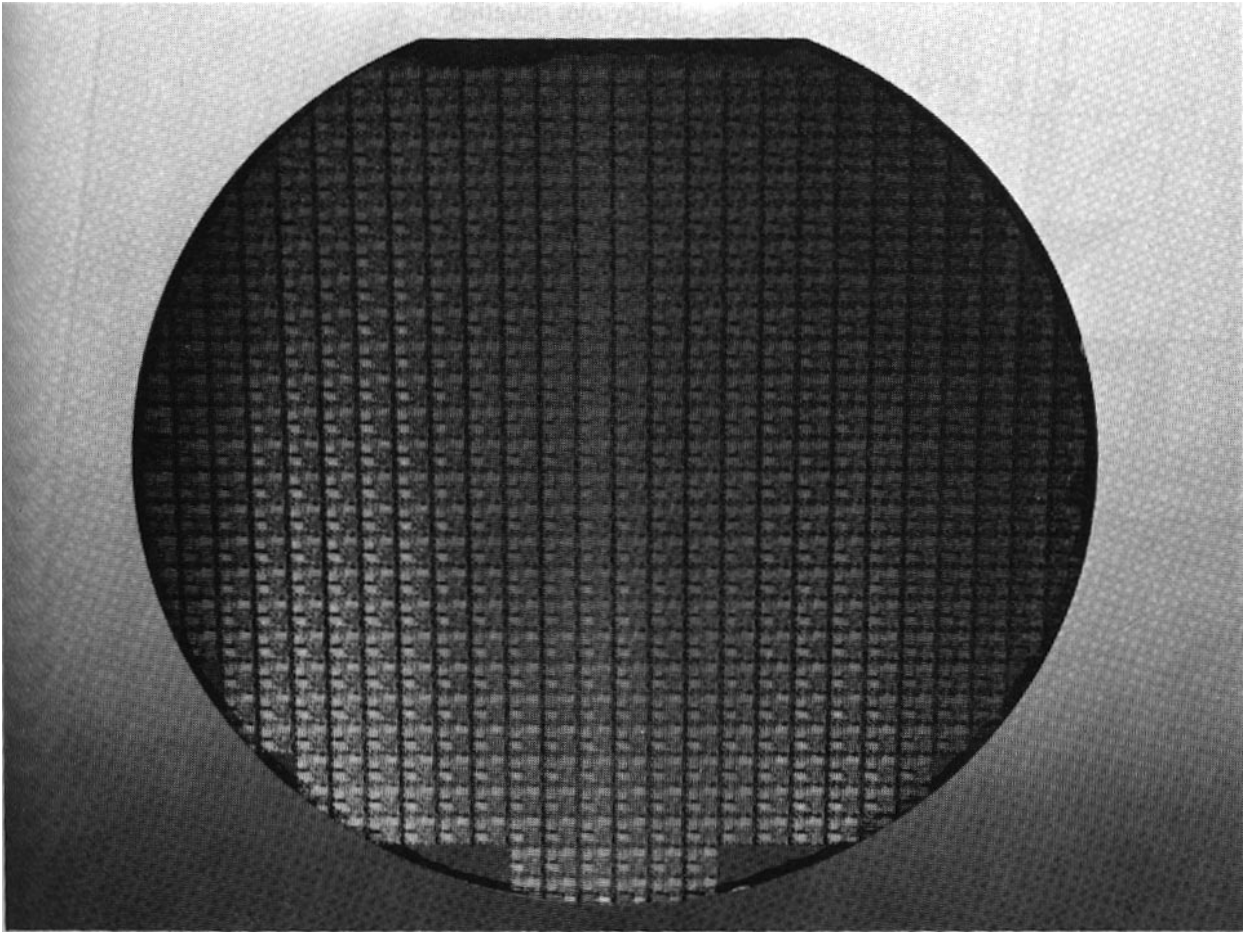
**Figure 17-19** *Comparison of a vacuum-tube rectifier with a solid-state counterpart. Such components allowed substantial miniaturization in the early days of solid-state technology. (Courtesy of R. S. Wortman.)*



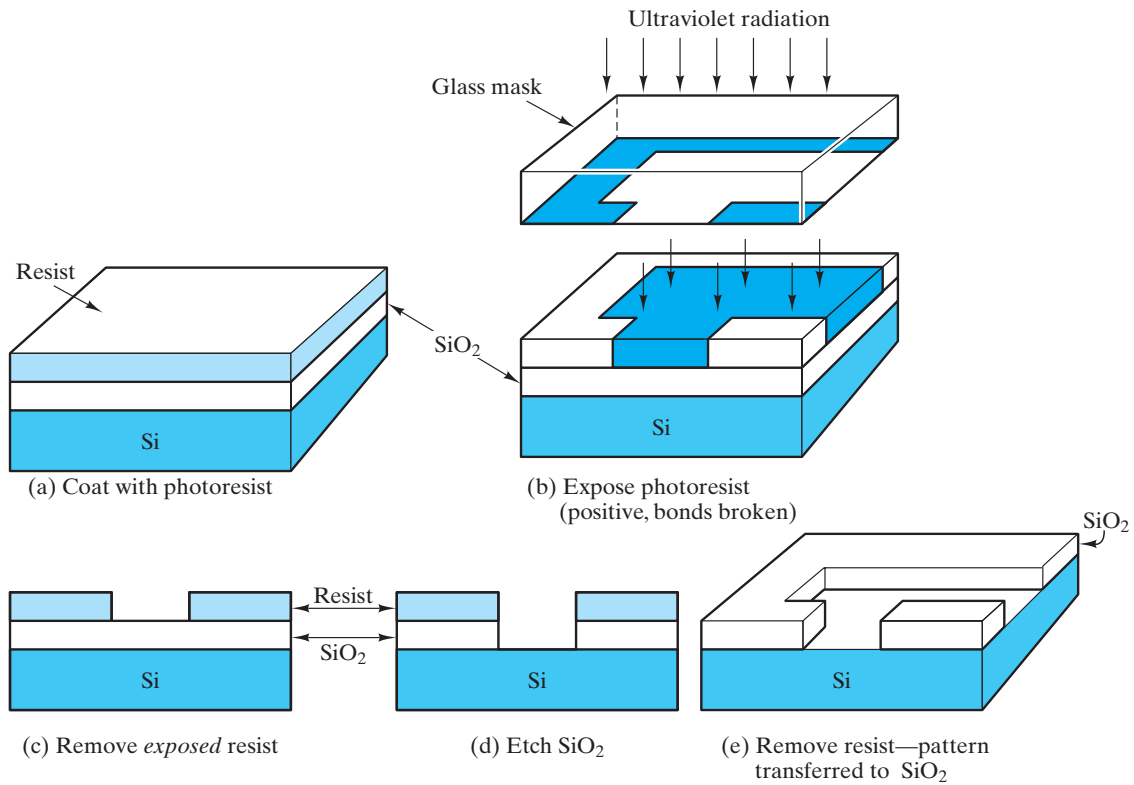
**Figure 17-20** Schematic of a transistor (a  $p$ - $n$ - $p$  sandwich). The overshoot of electron holes across the base ( $n$ -type region) is an exponential function of the emitter voltage,  $V_e$ . Because the collector current ( $I_c$ ) is similarly an exponential function of  $V_e$ , this device serves as an amplifier. An  $n$ - $p$ - $n$  transistor functions similarly except that electrons rather than holes are the overall current source.



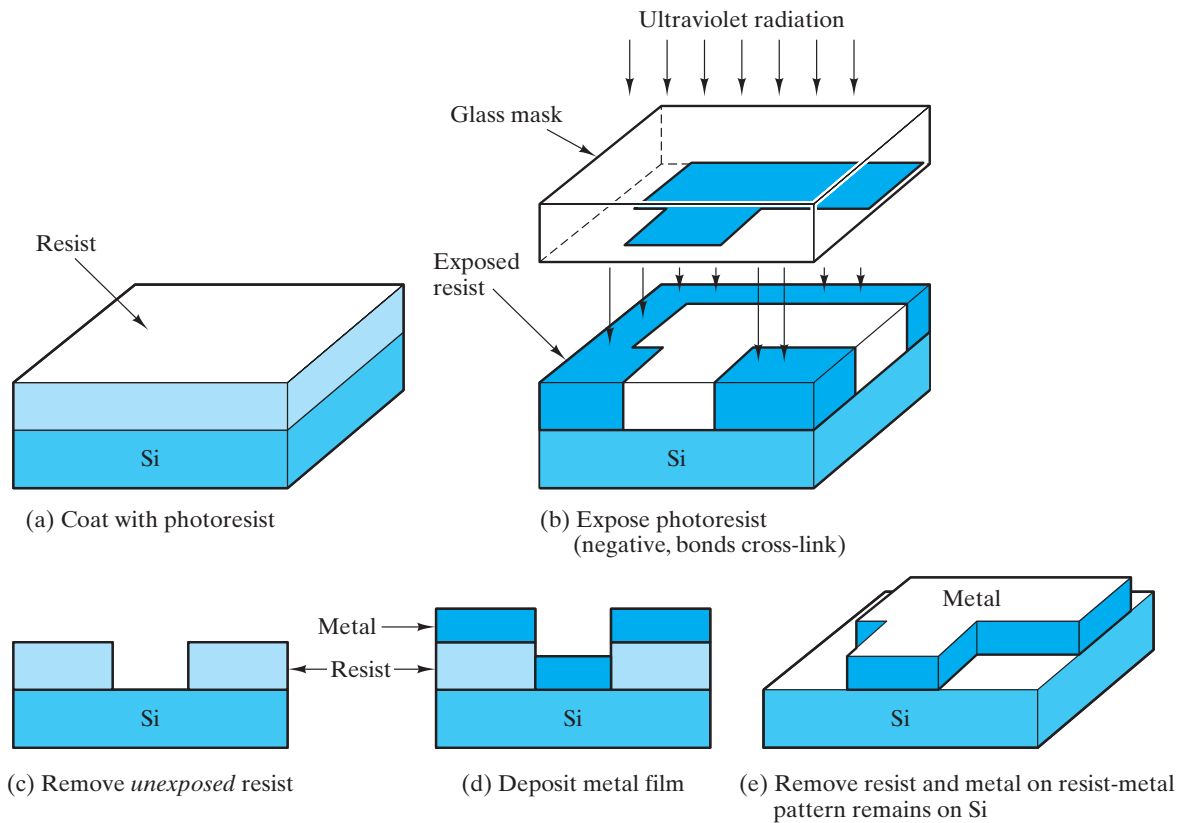
**Figure 17-21** Schematic of a field-effect transistor (FET). A negative voltage applied to the gate produces a field under the vitreous silica layer and a resulting p-type conductive channel between the source and the drain. The width of the gate is less than 1  $\mu\text{m}$  in contemporary integrated circuits.



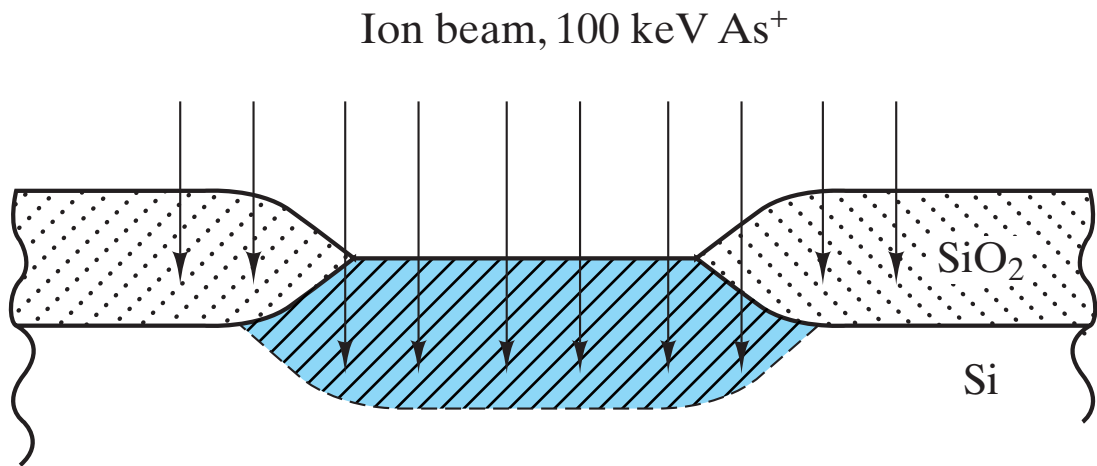
**Figure 17-22** *A silicon wafer (1.5 mm thick  $\times$  150 mm diameter) containing numerous chips of the type illustrated in Figure 1-17. (Courtesy of R. D. Pashley, Intel Corporation)*



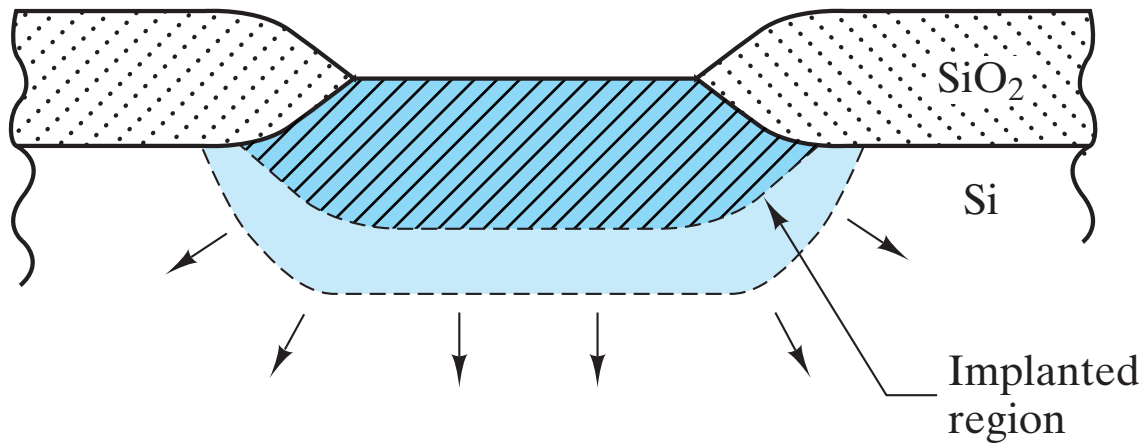
**Figure 17-23** Schematic illustration of the lithography process steps for producing vitreous  $\text{SiO}_2$  patterns on a silicon wafer. (From J. W. Mayer and S. S. Lau, *Electronic Materials Science: For Integrated Circuits in Si and GaAs*, Macmillan Publishing Company, New York, 1990.)



**Figure 17-24** Schematic illustration of the lithography process steps for producing metal patterns on a silicon wafer. (From J. W. Mayer and S. S. Lau, *Electronic Materials Science: For Integrated Circuits in Si and GaAs*, Macmillan Publishing Company, New York, 1990.)

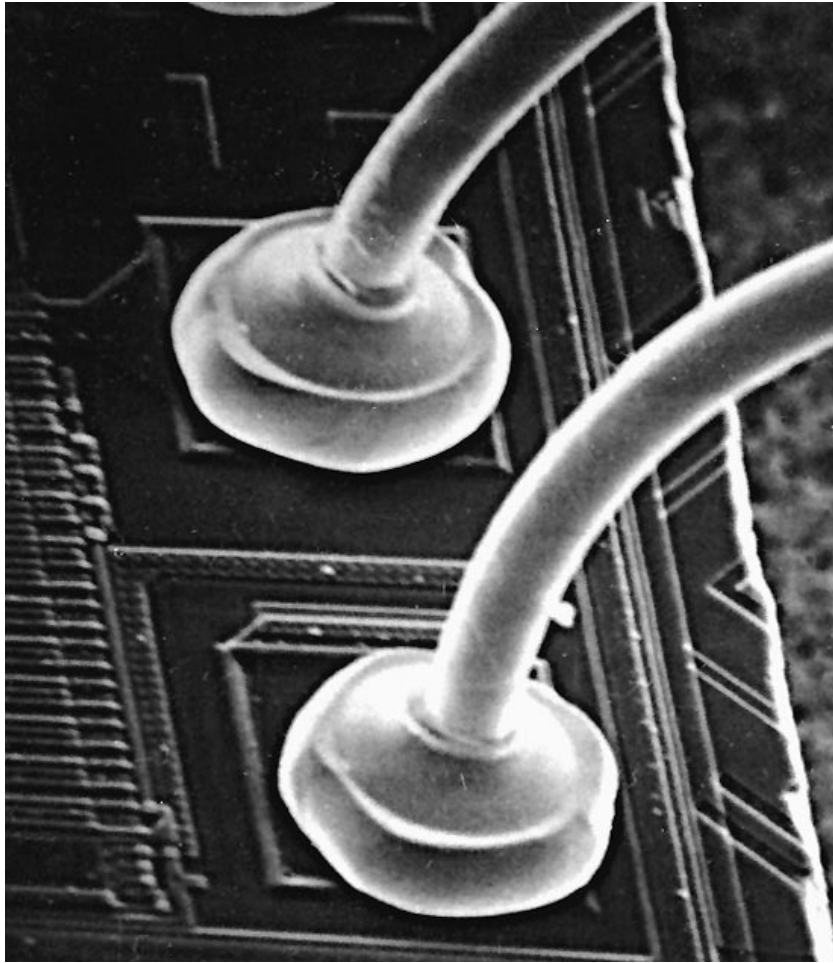


(a) Ion implantation of dopants (As).

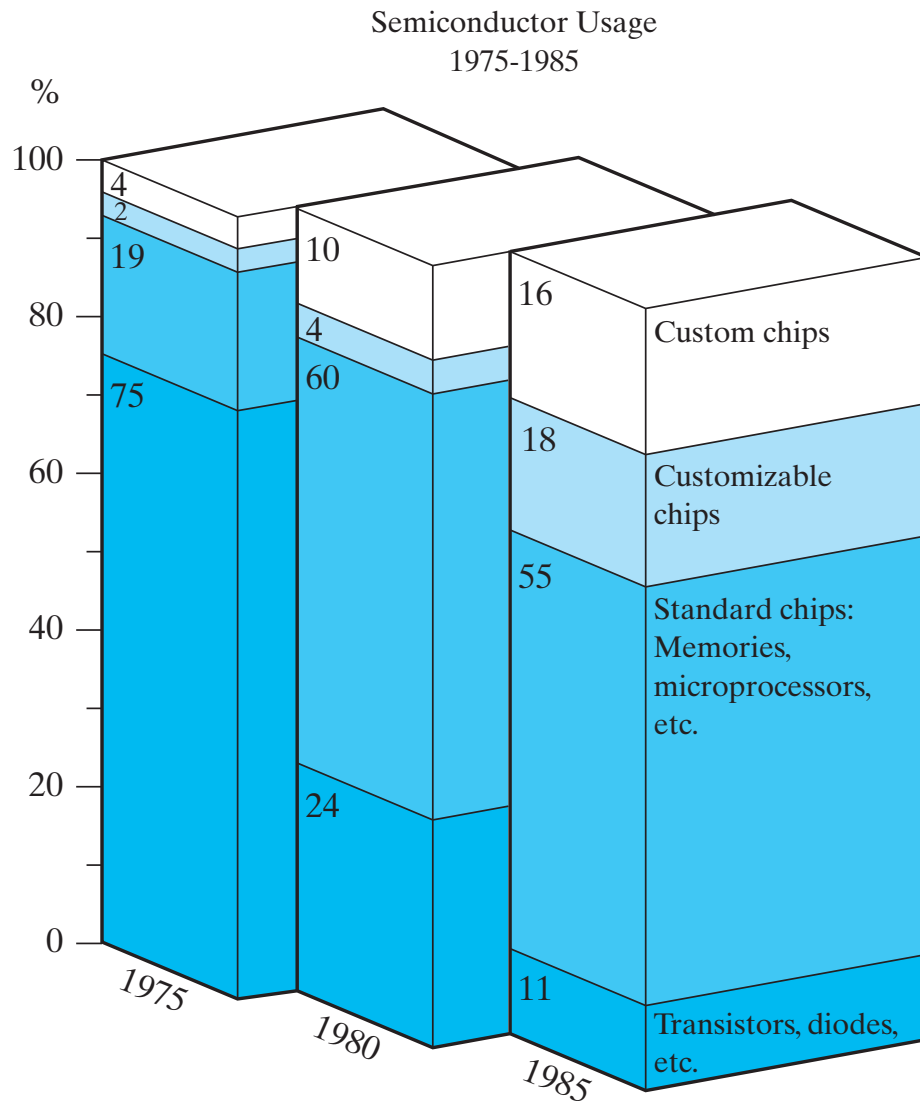


(b) Drive-in diffusion, 950-1050°C

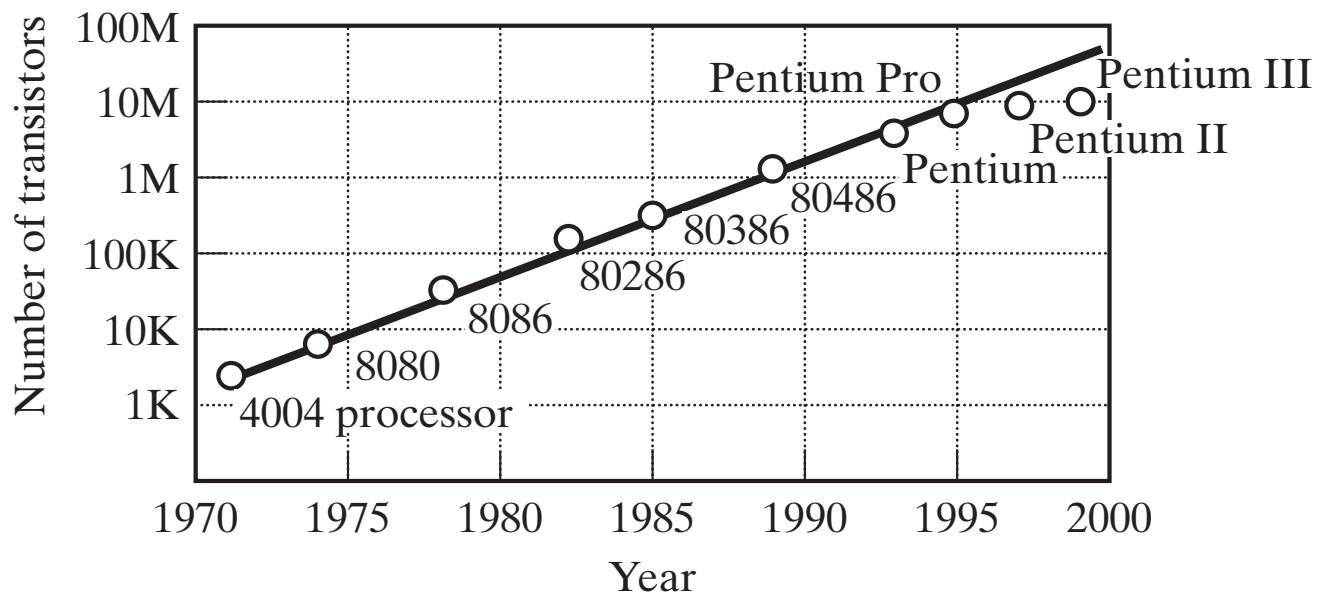
**Figure 17-25** Schematic illustration of the two-step doping of a silicon wafer with arsenic producing an n-type region beneath the vitreous  $\text{SiO}_2$  mask. (From J. W. Mayer and S. S. Lau, *Electronic Materials Science: For Integrated Circuits in Si and GaAs*, Macmillan Publishing Company, New York, 1990.)



**Figure 17-26** *Typical metal wire bond to an integrated circuit. (From C. Woychik and R. Senger, in Principles of Electronic Packaging, D. P. Seraphim, R. C. Lasky, and C.-Y. Li, Eds., McGraw-Hill Book Company, New York, 1989.)*



**Figure 17-27** Although separate solid-state elements such as transistors and diodes (e.g., Figure 17-19) provide miniaturization compared with vacuum tubes, microcircuits (e.g., Figure 1-17) allow substantially greater size reduction. The trend in which industry moved to microcircuit chips is shown here. Custom chips are those designed for specific applications. Standard chips represent more general-purpose circuit designs. Customizable chips are produced partway like standard chips but, in final stages, are prepared for specific circuit applications. There can be a fivefold difference in cost between a fully custom chip and a standard one. (Courtesy of the San Francisco Examiner, based on data provided by the Digital Equipment Corporation)



**Figure 17-28** *The rapid and steady growth in the number of transistors contained on a single microcircuit chip has generally followed Moore's law, which states that the number doubles roughly every two years. (After data from Intel Corporation)*

THE  
LONDON, EDINBURGH, AND DUBLIN  
PHILOSOPHICAL MAGAZINE  
• AND  
JOURNAL OF SCIENCE.

---

[FIFTH SERIES.]

---

OCTOBER 1897.

---

XI. *Cathode Rays.* By J. J. THOMSON, M.A., F.R.S.,  
*Cavendish Professor of Experimental Physics, Cambridge\*.*

THE experiments † discussed in this paper were undertaken in the hope of gaining some information as to the nature of the Cathode Rays. The most diverse opinions are held as to these rays; according to the almost unanimous opinion of German physicists they are due to some process in the æther to which—inasmuch as in a uniform magnetic field their course is circular and not rectilinear—no phenomenon hitherto observed is analogous: another view of these rays is that, so far from being wholly ætherial, they are in fact

(Courtesy of the Philosophical Magazine)



*Andrew Grove, Robert Noyce, and Gordon Moore  
in 1975. (Courtesy of Intel Corporation)*